Abstracts

High-Speed GaAs SDFL Divider Circuit

E.R. Walton, Jr., E.K. Shen, F.S. Lee, R. Zucca, Y.-D. Shen, B.M. Welch and R. Dikshit. "High-Speed GaAs SDFL Divider Circuit." 1982 Transactions on Microwave Theory and Techniques 30.7 (Jul. 1982 [T-MTT] (Joint Special Issue on GaAs IC's)): 1020-1026.

High-speed divider circuits find numerous applications in prescalers for counters, frequency synthesizers, and digital phase locked loops. To accommodate these applications, a high-speed multimode divider circuit has been designed, fabricated, and tested. This circuit, fabricated on semi-insulating Gallium Arsenide substrates, and utilizing Schottky diode FET logic (SDFL) technology, has been tested at a maximum clock frequency of 1.84 GHz. High yields of circuits operating over 1 GHz have been obtained over a number of wafers.

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